A New High-Level Synthesis Methodology of Cascaded Continuous-Time ΣΔ Modulators

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***Abstract*—This brief presents an efficient method for synthesizing cascaded sigma–delta modulators implemented with continuous-time circuits. It is based on the direct synthesis of the whole cascaded architecture in the continuous-time domain instead of using a discrete-to-continuous time transformation as has been done in previous approaches. In addition to placing the zeroes of the loop filter in an optimum way, the proposed methodology leads to more efficient architectures in terms of circuitry complexity, power consumption and robustness with respect to circuit errors.**

***Index Terms*—Analog–digital conversion, continuous-time sigma–delta (ΣΔ) modulation.**

I. Introduction

CONTINUOUS-TIME (CT) sigma–delta modulators (ΣΔMs) are suited to analog-to-digital (A/D) interfaces in submicrometer CMOS [1]. Although most ΣΔMs employ discrete-time (DT) circuits, CT techniques are applicable to broadband data communication systems due, among other features, to their intrinsic anti-aliasing filtering and their suitability for fast operation with low power consumption [2], [3].

Compared to DT-ΣΔMs, a drawback of CT modulators is their higher sensitivity to some circuit errors, namely: clock jitter, excess loop delay and time constant tolerances [2], [3]. Among other things, the impact of these errors influences the choice of the architecture. Particularly, most reported CT-ΣΔM s ICs employ single-loop topologies [4], [5] to circumvent the larger impact of tolerances on cascaded architectures. However, some recent contributions demonstrate that cascaded CT-ΣΔM ICs are feasible and well suited to broadband applications [6]. This is significant because cascaded architectures have larger modularity and less stability problems than their single-loop counterparts for the same filtering order.

Different authors have addressed the synthesis of high-order cascaded CT-ΣΔMs [7]–[9]. In all cases, the proposed methods are based on applying a DT-to-CT transformation to an equivalent DT topology that fulfils the required specifications. In most cases, the use of such transformation yields an increase of the analog circuit complexity, with the subsequent penalty in silicon area, power consumption, and sensitivity to parameter variations.

Manuscript received May 13, 2005; revised October 26, 2005. This work was supported by the Spanish Ministry of Science and Education (with support from European Regional Development Fund) under Contract TEC2004-01752/MIC. This paper was recommended by Associate Editor H. Hashemi.

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Digital Object Identifier 10.1109/TCSII.2006.875310

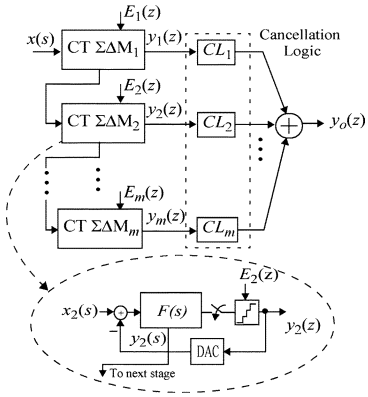

Fig. 1. Conceptual block diagram of a cascaded CT-ΣΔM

This brief presents a direct synthesis method for cascaded architectures. On the one hand, this method yields better placing of the noise transfer function zeroes and poles. On the other hand, it reduces the number of analog components. Thus, more robust and efficient architectures are obtained than when using DT-to-CT transformation. The method is illustrated in this brief through the synthesis of a 2-1-1-1 cascaded CT-ΣΔM for 12-bit at 40-MS/s.

II. Cascaded CT ΣΔ Modulators

Fig. 1 shows the conceptual block diagram of a m-stage cascaded CT-ΣΔM. Each stage, consisting of a single-loop CT-ΣΔM (typically either second or first order), modulates a signal that contains the quantization error generated in the previous stage. Once in the digital domain, the stage outputs (y_i) are processed and combined by the cancellation logic so that only the quantization error of the last stage remains. Also, this error is shaped by a transfer function whose order equals the sum of the respective orders of all the stages in the cascade.

Cascaded CT-ΣΔMs are typically synthesized from equivalent DT systems and use the same digital cancellation logic [8] as the DT prototype. This DT-to-CT equivalence can be guaranteed because at each stage the corresponding feedback transfer function from the quantizer output to the quantizer input is of discrete-time nature [2]. Assuming a rectangular impulsive response at the digital-to-analog converter (DAC), this equivalent DT loop filter transfer function is calculated as [10], [11]

$$F(z) = \sum_{p_i} \mathrm{Re}\left(\frac{F(s)}{s} \cdot \frac{e^{m_1 T_s \cdot s}}{z - e^{T_s \cdot s}}\right) - \sum_{p_i} \mathrm{Re}\left(\frac{F(s)}{s} \cdot \frac{e^{m_2 T_s \cdot s}}{z - e^{T_s \cdot s}}\right) \quad (1)$$

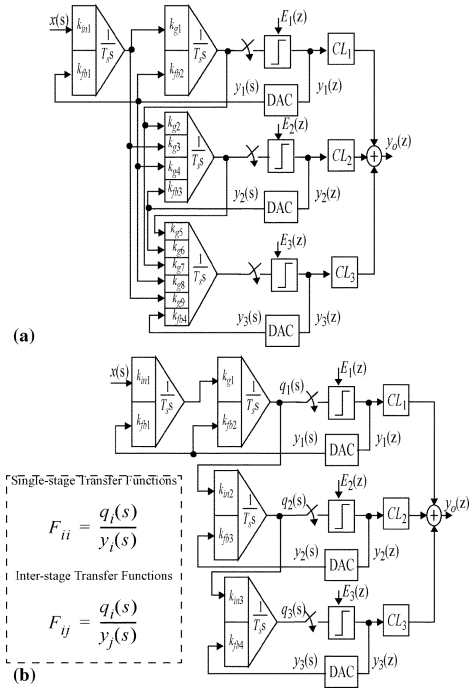

Fig. 2. Cascaded 2-1-1 CT $\Sigma\Delta$M architecture obtained (a) from an equivalent DT $\Sigma\Delta$M, and (b) using the proposed method.

where $f_s = 1/T_s$ is the sampling frequency; $m_1 = 1 - t_d/T_s$; $m_2 = 1 - (t_d + \tau)/T_s$; t_d, and τ are, respectively, the time delay and pulsewidth of the DAC waveform; p_i are the poles of $F(s)/s$ and $\mathrm{Re}(x)$ stands for the residue of x.

To get a functional CT-$\Sigma\Delta$M whose cancellation logic coincides with that of the original DT-$\Sigma\Delta$M, every state variable and DAC output must be connected to the integrator input of the ulterior stages in the cascade [8]. This increases the number of analog components (transconductors, amplifiers, and DACs) needed. For instance, Fig. 2(a) shows a cascaded 2-1-1 CT-$\Sigma\Delta$M obtained from an existing DT-$\Sigma\Delta$M [12]. Note that eight scaling coefficients (k_{g2-9}) and their corresponding signal paths are needed to connect the different stages of the modulator. As a counterpart, if the CT-$\Sigma\Delta$M is directly synthesized by following the technique in this brief, the number of integrating paths can be reduced—see Fig. 2(b).

III. Proposed Methodology

Let us consider the more general case of the m-stage cascaded CT-$\Sigma\Delta$M shown in Fig. 1. The overall output y_o is given by

$$y_o(z) = \sum_{k=1}^{m} y_k(z) CL_k(z) \tag{2}$$

where $y_k(z)$ and $CL_k(z)$ denote, respectively, the output and the cancellation transfer function of the kth stage.

If the modulator input $x(t)$ is set to zero, the output of each stage can be written as

$$y_k(z) = \frac{E_k(z) + \sum_{i=1}^{k-1} Z\left\{ L^{-1}[H_D F_{ik}]\big|_{nT_s} \right\} y_i(z)}{1 - Z\left\{ L^{-1}[H_D F_{kk}]\big|_{nT_s} \right\}} \tag{3}$$

where Z stands for the z-transform, L^{-1} is the inverse Laplace transform, $H_D \equiv H_{DAC}(s)$ is the DAC transfer function, and

$$F_{ij} = F_{ij}(s) = \frac{\text{Input Quantizer j}}{y_i(s)} \tag{4}$$

represents the transfer function from $y_i(s)$ to the input of the jth quantizer [see Fig. 2(b)].

Using the notation $Z(L^{-1}(H_D F_{km})|_{nT_S}) \equiv Z_{km}$, the output of each stage is given by

$$y_k(z) = \frac{E_k(z)}{1 - Z_{kk}} + \sum_{i=1}^{k-1} \frac{Z_{ik} y_i(z)}{1 - Z_{kk}} \tag{5}$$

and the output of the modulator can be written as

$$y_o = \sum_{k=1}^{m} y_k CL_k = \sum_{k=1}^{m} \left(\frac{E_k}{1 - Z_{kk}} + \frac{1}{1 - Z_{kk}} \sum_{i=1}^{k-1} Z_{ik} y_i \right) CL_k. \tag{6}$$

The cancellation logic transfer function CL_k is calculated by annulling the quantization errors of the first $m-1$ stages. This gives

$$CL_k(z) = \frac{-Z_{km} CL_m}{1 - Z_{mm}} = \frac{-Z\left\{ L^{-1}[H_D F_{km}]\,|_{nT_s} \right\} CL_m(z)}{1 - Z\left\{ L^{-1}[H_D F_{mm}]\big|_{nT_s} \right\}} \tag{7}$$

where the cancellation logic transfer function of the last stage, $CL_m(z)$, can be chosen to be the simplest form that preserves the required noise shaping.

Note that the design equations (2)–(7) do not only take into account the single-stage loop filter transfer functions (F_{ii}), but also the inter-stage loop filter transfer functions $(F_{ij}, i \neq j)$. The latter are CT integrating paths appearing only when the modulator stages are connected to form the cascaded $\Sigma\Delta$M and must be included in the synthesis methodology to obtain a functional modulator with a minimum number of inter-stage paths.

Therefore, the following systematic procedure can be proposed for the synthesis of cascaded CT $\Sigma\Delta$Ms.[1]

- First, the poles of the single-loop transfer functions $(F_{ii}(s))$ are optimally placed in the signal bandwidth for given specifications. The poles of the individual stages can be placed such that the overall pole distribution within the signal bandwidth is equivalent to that proposed in [13].
- Secondly, each individual stage is optimized following a similar procedure as the one proposed in [14], that is, numerator coefficients in F_{ii} are optimized to maximize the resolution while maintaining the system stability. This process is carried out entirely in the CT domain and no equivalence to an existing DT modulator needs to be considered. Once F_{ii} are defined, $F_{ij}, i \neq j$ are automatically determined by the inter-stage integrating paths as outlined in Fig. 2(b).
- Thirdly, once the individual stages are designed, (7) is used to obtain the cancellation transfer functions.

[1]In this procedure, the modulator order, oversampling ratio, and number of bits of internal quantizers are assumed to be determined for the given specifications from well-known expressions [1].

For illustration, the 2-1-1 CT-ΣΔM of Fig. 2(b) was synthesized using (2)–(7) to achieve 16-bit resolution in a 750-kHz bandwidth, with a sampling frequency of 48 MHz (oversampling ratio $M = 32$) [12]. For simplicity, in order to facilitate the comparison of the performance of both modulators in Fig. 2, the coefficients of the first stage $(k_{in1}, k_{g1}, k_{fb1}, k_{fb2})$ are taken to be equal in both systems and are obtained from a DT-to-CT transformation of the first stage of the DT-ΣΔM in [12]. The rest of the coefficients in Fig. 2(b) are chosen such that the time constant of the integrators is the inverse of the sampling frequency $(T_s = 1/f_s)$. In summary

$$\begin{aligned} k_{in1} &= -k_{fb1} = 1/4 \\ k_{fb2} &= -3/8 \\ k_{g1} &= k_{in2} = -k_{fb3} = k_{in3} = -k_{fb4} = 1. \end{aligned} \tag{8}$$

Thus, the single-loop and inter-stage transfer functions are

$$\begin{aligned} F_{11} &= \frac{-\left(\frac{3T_s}{8}s + \frac{1}{4}\right)}{(sT_s)^2} \\ F_{22} &= F_{33} = \frac{-1}{sT_s} \\ F_{13} &= \frac{-\left(\frac{3T_s}{8}s + \frac{1}{4}\right)}{(sT_s)^4} \\ F_{23} &= \frac{-1}{(sT_s)^2} \end{aligned} \tag{9}$$

and the cancellation logic transfer functions can be calculated using (7)–(9). Considering a nonreturn-to-zero (NRZ) DAC, the following are obtained:

$$\begin{aligned} CL_1 &= \frac{z^{-1}}{48}(7 + 29z^{-1} - 7z^{-2} - 5z^{-3}) \\ CL_2 &= z^{-1}(1 + z^{-1})(1 - z^{-1})^2 \\ CL_3 &= 2(1 - z^{-1})^3 \end{aligned} \tag{10}$$

where CL_3 is chosen to have three zeroes at dc, corresponding to the zeroes contributed by the first three integrators.

To compare the robustness of both modulators in Fig. 2, the effect of mismatch on the signal-to-noise ratio (SNR) was simulated using SIMSIDES—a SIMULINK-based time-domain behavioral simulator for ΣΔMs [15]. For this purpose, maximum values of mismatch were estimated for a 0.18-μm CMOS technology. On the one hand, capacitor mismatch (σ_C) lower than 1% are standard in modern technologies. On the other hand, MOS transconductance mismatch (σ_{gm}) is related to drain current mismatch (σ_{I_d}) by the following expression:

$$2\sigma_{g_m}/g_m = \sigma_{I_d}/I_d. \tag{11}$$

In the case of the 0.18-μm technology addressed, assuming typical transistor sizes and a maximum spacing between transistors of 1500 μm, a maximum $\sigma_{I_d}/I_d \leq 2\%$ is obtained. Then, taking into account that in a linearized transconductor, a minimum of 4 transconductance elements are used and that the tuning circuit introduces an additional error, maximum values of $\sigma_{g_m}/g_m \leq 2.5\%$ are expected.

Both modulators in Fig. 2 were simulated considering a G_m–C implementation. The results are shown in Fig. 3, where the SNR loss is represented as a function of σ_{gm} and σ_C. For each point of these surfaces, 150 simulations were carried out using random variations with the corresponding standard deviations. The value of the SNR loss represented in Fig. 3 stands for the difference between the ideal SNR, i.e., with no parameter variation, and the SNR with 90% of the 150 simulations above it. It is shown that the lower analog component count in Fig. 2(b) is reflected in a lower variance of the modulator coefficients, leading to better behavior in terms of sensitivity to mismatch.

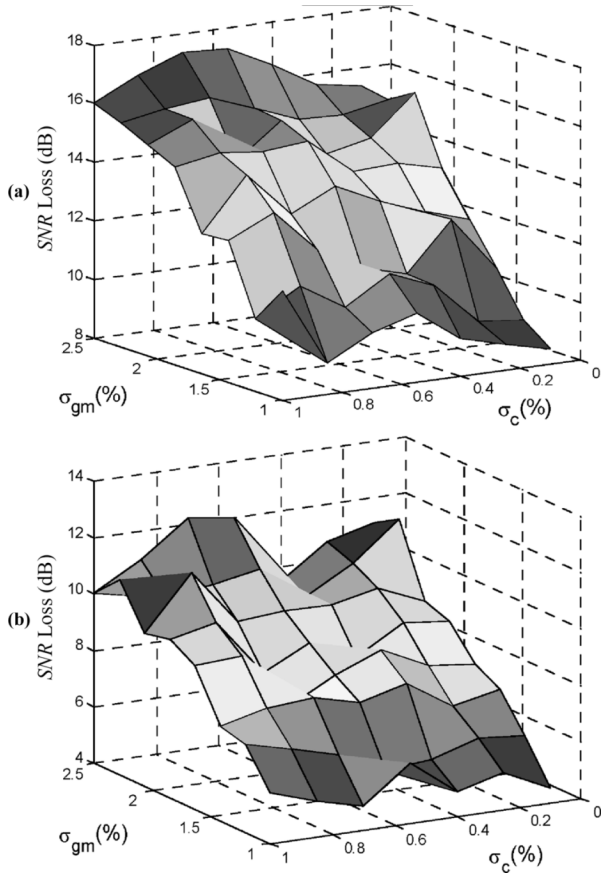

Fig. 3. Effect of mismatch on the SNR of a cascaded 2-1-1 CT ΣΔM obtained: (a) from an equivalent DT ΣΔM, and (b) from the proposed method.

The same reasoning can be applied to the requirements in terms of dc gain of the transconductors. Since the number of transconductors connected to the same node is higher in the previous method, the equivalent impedance associated with these nodes tends to be lower and the requirement in terms of the individual transconductor output impedance is higher. Therefore, a higher dc gain is needed. Fig. 4 illustrates this point. Note that the SNR-peak starts dropping at a dc gain ≅ 5 dB higher in the case of the system designed following the previous method. For high dc gains, the two curves collide because the effect of this error becomes negligible.

IV. Synthesis Example

As an application of the proposed methodology, the 2-1-1-1 cascaded CT ΣΔM shown in Fig. 5 was synthesized to achieve 12-bit resolution within a 20-MHz signal bandwidth. In order to fulfill these specifications without being limited by the clock jitter error, the sampling frequency, f_s, and the number of bits of

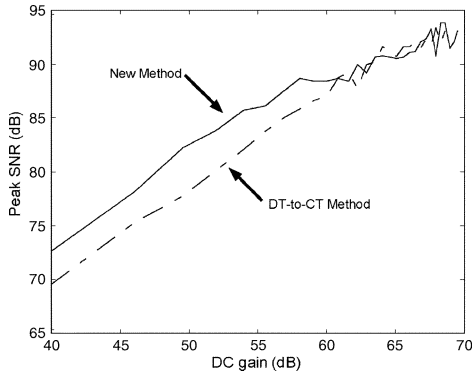

Fig. 4. Effect of dc gain on the SNR-peak.

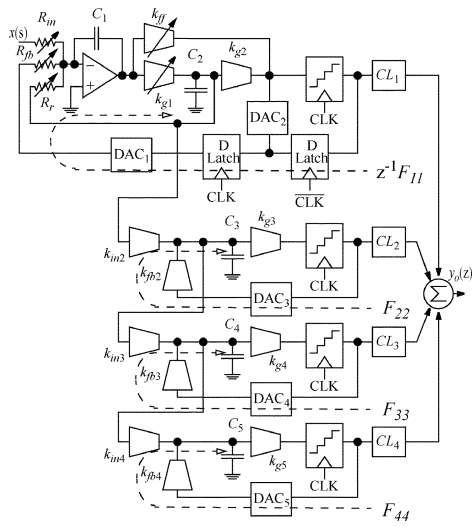

Fig. 5. Cascaded 2-1-1-1 CT $\Sigma\Delta$M.

the internal quantizers (and DACs), B, must be properly chosen. In the case of a fifth-order modulator like the one shown in Fig. 5, the in-band jitter noise power is minimized for $f_s = 240$ MHz and $B = 4$ [16].

Another critical source of error in CT $\Sigma\Delta$Ms is the excess loop delay. As shown in [17], this error can be compensated for by adding an extra feedback branch between the output and the input to the quantizer (DAC_2 in Fig. 5) and two D-latches. By adding this extra branch with the appropriate gain, the loop impulse response is exactly the same as that of the original. This extra feedback term can be easily included in the calculation of the cancellation logic by modifying appropriately the F_{ij} transfer functions. In practice, this extra feedback branch will only affect the cancellation logic if the input to other stages is tapped at quantizer inputs or if the last stage includes a second DAC. In a practical implementation it might be advantageous to make DAC_2 programmable [5].

Considering the factors above, the 2-1-1-1 architecture in Fig. 5 was synthesized using the methodology described in Section III. The first stage is formed by a resonator which has its pole placed at $\omega_p = 2\pi\sqrt{7/9}B_w$, minimizing the quantization noise transfer function in the signal bandwidth, B_w. Resistor variations can be tuned out using a combination of a discrete rough tuning of the resistors (R_{in}, R_{fb} and R_r) and a continuous fine tuning of the transconductors k_{ff} and k_{g1}. This tuning can be also used

TABLE I
MODULATOR DESIGN VALUES

Parameter	Value
R_{in}, R_{fb}	1kΩ
R_r	2.9kΩ
$k_{g2} \ldots k_{g5}$	50μA/V
k_{g1}	500μA/V
k_{ff}	120μA/V
$k_{in2} \ldots k_{in4}, -k_{fb2} \ldots -k_{fb4}$	450μA/V
C_1	7.5pF
$C_2 \ldots C_5$	1.875pF

to cancel the effect of finite gain-bandwidth product (GB) of the front-end opamp, due to the fact that this error can be modelled as an integrator gain error [5]. All the other transconductors could be tuned in order to keep the time constant C/g_m unchanged over C variations. In this case, the single-loop and inter-stage transfer functions are

$$\begin{aligned} F_{11} &= -\frac{b_{11}s + b_{10}}{s^2 + \omega_p^2} \\ F_{ii} &= \frac{-1}{T_s s}, \qquad i = 2, 3, 4 \\ F_{14} &= -\frac{b'_{10}}{(T_s s)^3 \left(s^2 + \omega_p^2\right)} \\ F_{24} &= \frac{-1}{(T_s s)^3} \\ F_{34} &= \frac{-1}{(T_s s)^2} \end{aligned} \tag{12}$$

where

$$\omega_p = \sqrt{\frac{k_{g1}}{R_r C_1 C_2}} \tag{13}$$

and coefficients b_{11}, b_{10}, and b'_{10} are given by

$$b_{11} = \frac{k_{ff}}{R_{fb} C_1}; \quad b_{10} = \frac{k_{g1} k_{g2}}{R_{fb} C_1 C_2}; \quad b'_{10} = \frac{k_{g1}}{R_{fb} C_1 C_2}. \tag{14}$$

These coefficients are found through an iterative simulation-based process that optimizes the first stage of the modulator in order to maximize the SNR while maintaining stability. The outcome of this process—done entirely in the CT domain—is summarized in Table I. This table includes the values of loop filter coefficients, k_i (implemented as transconductances) as well as the capacitances, C_i, and resistances, R_i obtained from the optimization process. The expressions of CL_i, can be obtained from (7) and (12), giving

$$\begin{aligned} CL_1 &= -z^{-1}(n_{14} + n_{13}z^{-1} + n_{12}z^{-2} \\ &\qquad + n_{11}z^{-3} + n_{10}z^{-4}) \\ CL_2 &= \frac{1}{6}z^{-1}(1 + 4z^{-1} + z^{-1}) \\ &\qquad \times \left(1 - 2\cos(T_s\omega_p)z^{-1} + z^{-2}\right) \\ CL_3 &= \frac{1}{2}z^{-1}(1 + z^{-1})(1 - z^{-1}) \\ &\qquad \times \left(1 - 2\cos(T_s\omega_p)z^{-1} + z^{-2}\right) \\ CL_4 &= (1 - z^{-1})^2 \left(1 - 2\cos(T_s\omega_p)z^{-1} + z^{-2}\right) \end{aligned} \tag{15}$$

TABLE II
NONIDEALITIES CONSIDERED IN THE SIMULATION

Front-end opamp	
GB	600 MHz
DC Gain	70 dB
Phase Margin	60°
Parasitic Input Capacitance	0.2 pF
Parasitic Output Capacitance	0.2 pF
Differential Output Swing	0.5 V
Resistors HD3	78 dBV
Transconductors	
DC Gain	50 dB
Differential Input Amplitude	0.3 V
Differential Output Amplitude	0.3 V
HD3	56 dBV

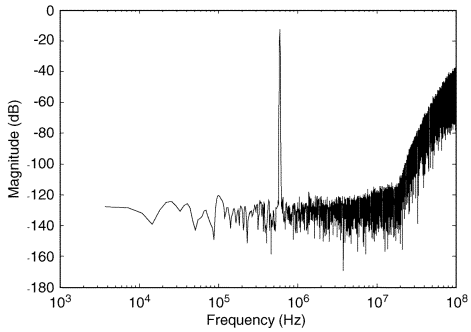

Fig. 6. Output spectrum of the 2-1-1-1 CT ΣΔM in Fig. 5.

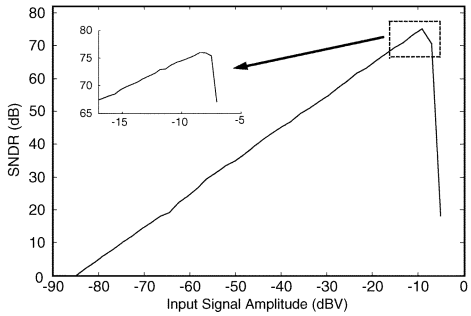

Fig. 7. SNDR versus input amplitude.

where coefficients n_{ij} are given by

$$n_{10} = n_{14} = \frac{-b'_{10}}{T_s^3\omega_p^5}\left[\sin(T_s\omega_p) - T_s\omega_p + \frac{1}{6}(T_s\omega_p)^3\right]$$
$$n_{11} = n_{13} = \frac{-b'_{10}}{T_s^3\omega_p^5}\left[(T_s\omega_p)^3\frac{2-\cos(T_s\omega_p)}{3} - 4\sin(T_s\omega_p) + 2T_s\omega_p\left(\cos(T_s\omega_p)+1\right)\right]$$
$$n_{12} = \frac{-b'_{10}}{T_s^3\omega_p^5}\left[(T_s\omega_p)^3\frac{1-4\cos(T_s\omega_p)}{3} + 6\sin(T_s\omega_p) - 2T_s\omega_p\left(1+2\cos(T_s\omega_p)\right)\right] \quad (16)$$

The modulator in Fig. 5 was simulated using SIMSIDES, taking into account the non-ideal effects listed in Table II. Fig. 6 shows an output spectrum for a −8 dBV@6-MHz sinewave signal, demonstrating a correct operation within the signal bandwidth. The effective resolution is 76 dB (12.4 bits) as shown in Fig. 7, where the signal-to-noise-plus-distortion ratio (SNDR) is plotted as a function of the input signal amplitude.

V. CONCLUSION

This brief presents a new methodology for synthesizing cascaded continuous-time ΣΔMs. The resulting circuits are less complex and more robust than those obtained with conventional methodologies. Examples supported by realistic behavioral simulations are given to validate the presented approach.

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